JANUS Jumper Settings

Position	Description	Signals	Jumper open	Jumper set
JP10	I2C BYPAS	SSCK – I2CSCK	CPLD Pin 1 to CODEC Pin 24 SCLK	CODEC Direct connect via R34 Pull-up –> CPLD Pin 39 –> Atlas A20 I2CSCK
JP11	I2C BYPAS	MOSI – I2CSDA	CPLD Pin 100 to CODEC Pin 23 SDIN	CODEC direct connect via R37 pull-up –> CPLD Pin 37 –> Atlas A21 I2CSDA
JP12	LAST JTAG	CTDO – SDOBACK		A25 to A27; Programming through Atlas/OZY; JANUS/OZY next to each other; OZY upstream
JP2/JP5	Signal input level		High I/Q input amplitude	Low I/Q input amplitude
JP4/JP1	BAL - UNBAL		Balanced I/Q input	Unbalanced I/Q input
JP6/JP3	BAL - UNBAL		Balanced I/Q input	Unbalanced I/Q input
JP7	MIC BIAS		No bias voltage	Bias voltage to tip (2-3) or ring (2-1)
JP8	PTT		No PTT	PTT to tip (2-3) or ring (2-1)
JP9	MIC AUDIO		No open allowed	Mike audio to tip (2-3) or ring (2-1)
TP1	Both pins connected to GND			
TP2	Both pins connected to GNDA			
TP3	CPLD Pin 88 – EXP4			
TP4	Both pins connected to GNDA			
10.05.07	DL6KBF			