OZY Headers and Jumper Settings

			RED indicates default setting		
Position	**Device**	**Description**	**Jumper OPEN**	**Jumper SET 1-2**	**Jumper SET 1-3**
HDR1	2x5pin Header	JTAG Active Serial Device U1 configuration			
HDR2	2x5pin Header	JTAG FPGA configuration			
J01	2pin header	CLK3 LVDS RX			
J02	2pin header	CLK2 LVDS RX			
J03	2pin header	CLKX LVDS TX			
J04	2pin header	CLKY LVDS TX			
J05	2pin header	External I2C connector	1 = SCL; 2=SDA		
J06	2x5pin Header	RS232 connector; 1=RS232_RxD0, 2= RS232_RxD2, 3=RS232_TxD0, 4=RS232_TxD2, 5+6+7+8+9+10=GND			
J07	2pin header	External RESET		Reset	
J08	DB9F	Serial Port to SDR1000			
J10	0603	FPGA_CLK5		Optional XTAL clocks Enable	
J11	0603	FPGA_CLK4		Optional XTAL clocks Enable	
J12	0603	LVDS RX Enable			
J13	0603	LVDS TX Enable			
J9/J16/J18 /J19/J22	0603	Connect J8 to ULN2003 (1-3) or to 74ACT541 (1-2)			
J17	2x10pin Header	GPIO connector			
J20	DB25F	Parallel Port to SDR1000			
J21	2pin header	Optional external clocks input connector; pin 1 = FPGA_CLK6, pin 2= FPGA_CLK7			
J23/J24	3pin Header	Programming configuration Jumper; table on board			
J25	0603	U13 OEPULLUP2 to GND	Output DISABLE U13 LCX541	Output ENABLE U13	
J26	0603	+3.3V Select from Bus (1-2) or U14 LD1117-3.3 (1-3)			
J27	0603	U4 I2C programming	FX2 programming	Atlas Pin 21 SDA	
J28	0603	U4 I2C programming	FX2 programming	Atlas Pin 20 SCL	
J29	0603	RESET through Atlas		RESET through Atlas A19	
J30	0603	U15 OEPULLUP1 to GND	Output DISABLE U15 ACT541	Output ENABLE U15	
J32	3pin Jumper	+5V Select	No OFF allowed	Pos 2-1: Bus powered	Pos 2-3: USB powered
TP18		FX2 CTL5			
TP19		FX2 CTL4			
TP20		FX2 CTL3			